Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently amended) A test apparatus comprising:

a substrate retainer for holding a substrate having a plurality of chips;

a probe card having an array of probes aligned in rows and columns, wherein each of the probes is for contacting respective chips of the substrate held by the retainer and each includes a plurality of probe needles;

a tester which conducts a test routine by generating test signals and by receiving and analyzing return signals;

a test head for sending the test signals from the tester to the probe card, and for sending the return signals from the probe card to the tester; and

a main controller comprising a test result database for storing test data analyzed by the tester~~, and~~ for executing a cleaning error detection program to determine whether the test data contains cleaning errors resulting from a lack of cleanliness of the probe needles of the probes, and a cleaning error database for storing sample test data containing cleaning errors, and wherein the cleaning error detection program compares the test data stored in the test result database and the sample test data stored in the cleaning error database.

2. (Cancelled)

3. (Currently amended) The apparatus according to claim ~~2~~ 1, wherein the cleaning error detection program determines that the test data contains cleaning errors when the number of chips having matches between the test data and the sample test data is at least a reference value.

4. (Original) The apparatus according to claim 1, wherein the cleaning error detection program determines that the test data contains cleaning errors by monitoring a number of times the test data associated with each of the respective probes indicates a chip failure in successive test routines.

5. (Currently amended) A test method, comprising:

loading a substrate having a plurality of chips on a substrate retainer;

contacting probes of a probe card with respective chips of the substrate, the probe card having an array of probes aligned in rows and columns, wherein each of the probes includes a plurality of probe needles;

conducting a test routine by transmitting test signals to the respective chips via the probes of the probe card, receiving return signals from the respective chips via the probes of the probe card, and analyzing return signals to determine if the respective chips are defective to obtain resultant test data;

storing the test data associated with each probe into a test result database; ~~and~~

executing a cleaning error detection program to determine whether the

test data contains cleaning errors resulting from a lack of cleanliness of the probe needles of the probes; and

storing the test data in a test result database, and storing sample test data containing cleaning errors in a cleaning error database, wherein the cleaning error detection program compares the test data stored in the test result database and the sample test data stored in the cleaning error database.

6. (Original) The method according to claim 5, further comprising:

cleaning the probe needles of the probes if the cleaning error detection program determines that the test data contains cleaning errors, and then loading a new substrate on the substrate retainer to conduct a new test sequence; and

loading a new substrate on the substrate retainer to conduct a new test sequence if the cleaning error detection program determines that the test data does not contain cleaning errors.

7. (Cancelled)

8. (Currently amended) The method according to claim ~~7~~ 5, wherein the cleaning error detection program determines that the test data contains cleaning errors when the number of chips having matches between the test data and the sample test data is at least a reference value.

9. (Original) The method according to claim 5, wherein the cleaning error detection program determines that the test data contains cleaning errors by monitoring a number of times the test data associated with each of the respective probes indicates a chip failure in successive test routines.